



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,852	10/22/2001	Ko-Yan Shih	JCLA7022	9319

7590 10/19/2005  
J.C. PATENTS, INC.  
SUITE 250  
4 VENTURE  
IRVINE, CA 92618

EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
----------	--------------

2138

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/039,852	Applicant(s) SHIH ET AL.	
	Examiner John P. Trimmings	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This office action is in response to the applicant's RCE and amendment dated 8/24/2005.

The applicant has amended Claims 1, 2 and 6.

Claims 1-11 are pending.

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/24/2005 has been entered.

### ***Response to Arguments***

2. Applicant's arguments filed 8/24/2005 have been fully considered but they are not persuasive. The examiner has determined that the limitation, "through a plurality of input lines", is broad enough to encompass the reference Crouch test pattern load, which uses a plurality of input lines to load patterns into the scan chains (see FIG. 1 where 7 lines are used, S\_SE, STDI, TSTADDR[1:0], MTM[2:0]). One may "provide a test pattern", as claimed in applicant Claim 1, according to Crouch using the 7 input

Art Unit: 2133

lines cited, because all 7 lines cited in Crouch are in fact "inputs" to the chip (see column 7 lines 26-32 of Crouch).

3. Also, argued by the applicant is that the registers 310, 312 and 314 of the invention are not serially connected to each other. Even though such a limitation is not stated in the claims, the examiner will respond to the argument. The examiner does not find support in the disclosure for this feature and therefore rejects such a limitation if it were submitted. In contrast to the applicant's argument, the disclosure has in fact claimed (in Claim 1) "sequentially configuring a plurality of registers with the test pattern". Such a feature is a well-known practice in the art for serially loading a scan chain. Based on the examiner's ordinary skill in the art, in the opinion of the examiner, the limitations stated in the claims in the application are consistent with a boundary scan system, and therefore may be serially connected to one another.

4. Next, the applicant argues that the reference Crouch does not teach a multiplexing finite state machine controller. But the examiner disagrees. The controller 10 of FIG.1 and 2 in Crouch performs loading of data in several states (under control of the core address and mode inputs) as per column 2 lines 14-43. These functions are well known in the art and are performed by state machines such as BISTs and other controllers such as in the Crouch reference.

5. Finally, the applicant argues that the reference does not teach that the core module under test is tested after the registers are configured with the test pattern. But the invention of Crouch does indeed perform the test after loading the scan chain as stated in the previous final rejection of the examiner. The examiner sees no other

purpose for the referenced invention other than testing core modules after loading pattern data, as is claimed by the applicant, and so the argument is rejected.

***Claim Rejections - 35 USC § 112***

6. Claims 1 and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The subject matter added to the subject claims is considered by the examiner as new matter, and as such is not supported by the Disclosure as originally presented. The only real reference to the "input" is page 7 lines 4-6 (reference 1) and also page 8 lines 15-18 (reference 2). Reference 1 is very broad in that it notes that the input pins are command and data. The examiner notes that "command or data" pins, in the context of the applicant's Disclosure (wherein on page 4 applicant incorporates by references both JTAG TAP and boundary scan prior art), is consistent with a 5-pin JTAG interface. Also, reference 2 only discloses one data input pin in a description of a data load through to IPA 406. Therefore, in light of one input pin as per reference 2 of the applicant's Disclosure, and a JTAG TAP context in the applicant's Disclosure as per reference 1, the examiner has determined that a serial loading JTAG interface is the only reasonable interpretation for the input pins, and so the amendment to the claims, "through a plurality of input pins" is beyond the scope of the original disclosure.

***Claim Rejections - 35 USC § 102***

7. Claims 1-11 are maintained as being rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al., U.S. Patent No. 5592493. See the examiner's action dated 2/25/2005.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John P Trimmings  
Examiner  
Art Unit 2133



ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY